SCHEME AND SYLLABUS
FOR

MASTER OF TECHNOLOGY

(ELECTRONICS & COMMUNICATION ENGINEERING)

REGULAR/PART TIME

(SEMESTER SYSTEM)

Admission Batch 2016

FACULTY OF ENGINEERING & TECHNOLOGY

PUNJABI UNIVERSITY, PATIALA

LIST OF CORE COURSES (ALL COURSES ARE COMPULSORY)

MEC-101 WIRELESS AND MOBILE DATA COMMUNICATION
MEC-102 OPTICAL COMMUNICATION SYSTEM
MEC-103 VLSI DESIGN
MEC-104 MICROCONTROLLERS AND EMBEDDED SYSTEMS
MEC-105 ADVANCED DIGITAL SIGNAL PROCESSING
MEC-106 RESEARCH METHODOLOGY

LIST OF DEPARTMENT ELECTIVE COURSES (ANY SIX COURSES TO BE OPTED)

MEC-201 ANTENNA SYSTEM ENGINEERING
MEC-202 DIGITAL IMAGE PROCESSING AND ANALYSIS
MEC-203 INFORMATION THEORY AND CODING
MEC-204 EMI AND EMC TECHNIQUES
MEC-205 SEMICONDUCTOR DEVICES AND MODELING
MEC-206 ARTIFICIAL NEURAL NETWORKS AND FUZZY SYSTEMS
MEC-207 MEMS AND MICROSYSTEMS TECHNOLOGY
MEC-208 TELECOMMUNICATION SWITCHING SYSTEMS AND NETWORKS
MEC-209 PROGRAMMABLE LOGIC CONTROLLER
MEC-210 NANOELECTRONICS DEVICES ENGINEERING
MEC-211 PARALLEL COMPUTING FUNDAMENTALS
MEC-212 SPEECH PROCESSING
MEC-213 COMPUTER SYSTEM ARCHITECTURE
MEC-214 MICROELECTRONICS TECHNOLOGY
MEC-215 ADVANCED DIGITAL SYSTEM DESIGN
MEC-216 ADVANCED MICROPROCESSORS AND INTERFACING
MEC-217 MULTIMEDIA COMPRESSION TECHNIQUES
MEC-218 MICROWAVE INTEGRATED CIRCUITS
MEC-219 GLOBAL TRACKING AND POSITIONING SYSTEMS
MEC-220 COMMUNICATION NETWORK SECURITY
MEC-221 RF SYSTEM DESIGN
MEC-222 DATA AND COMPUTER COMMUNICATION NETWORKS

LIST OF OPEN ELECTIVE COURSES (It is over and above the basic requirement for the award of M.Tech degree. Student can opt any number of courses from open elective list).

MICRO ECONOMIC ANALYSIS (M.A. BUSINESS ECONOMICS)
QUANTITATIVE TECHNIQUES (M.A. BUSINESS ECONOMICS)
THEORY AND PRACTICE OF WAR – I (M.A. DEFENCE & STRATEGIC STUDIES)
PROFESSIONAL PHOTOGRAPHY (B. TECH TV, FILM PRODUCTION AND MEDIA TECHNOLOGY)
EARLY HISTORY OF BUDDHISM (M.A. BUDDHIST STUDIES)
ORIGIN & DEVELOPMENT OF SIKHISM (M.A. BUDDHIST STUDIES)
PHILOSOPHICAL FOUNDATIONS OF EDUCATION (M.A. EDUCATION)
ENGLISH PHONETICS AND PHONOLOGY (M.A. ENGLISH)
ART AND CULTURAL HISTORY OF INDIA (M.A. FINE ARTS)
GROWTH & DEVELOPMENT OF PRINT MEDIA (M.A JOURNALISM AND MASS COMMUNICATION)
GURU NANAK DEV: METAPHYSICS & EPISTEMOLOGY (M.A. PHILOSOPHY)
INDIVIDUAL AND SOCIETY (M. A. SOCIAL WORK)
HUMAN GROWTH AND DEVELOPMENT (M. A. SOCIAL WORK)
WOMEN'S MOVEMENT IN INDIA (M.A. WOMEN'S STUDIES)
POSITIONAL ASTRONOMY (M.SC. ASTRONOMY & SPACE PHYSICS)

IN ADDITION TO ABOVE OPEN ELECTIVE SUBJECTS, STUDENT CAN OPT ANY OTHER SUBJECT OFFERED BY UNIVERSITY DEPARTMENTS WITH THE CONSENT OF ACD OF ECE DEPARTMENT.

SEMINAR AND MINOR PROJECT

MEC-301 ELECTRONICS ENGG. LAB
MEC-302 SELF STUDY & SEMINAR
MEC-303 PROJECT

DISSERTATION

MEC-401 DISSERTATION

Instructions to the External Paper Setters for End Semester Theory examination

(Common for M.Tech. in Computer Engineering, Electronics and Communication Engineering, Mechanical Engineering Branches)

The M. Tech paper structure will be as shown below:

Pattern of Question Paper for End Semester Exam

TITLE OF SUBJECT (CODE----)

Master of Technology (Branch) …….. TIME ALLOWED: 3 Hour

Roll. No……. Maximum Marks: 50

Note:- Attempt any three questions from section A and any three questions from section B. All questions of Section C are compulsory.

Section-A (From Section A of the syllabus)

Q1.
Q2.
Q3.
Q4.
Q5.

3x5

Section-B (From Section B of the syllabus)

Q6.
Q7.
Q8.
Q9.
Q10. 3x5

Section-C (Ten short/objective questions) (From Whole of the Syllabus uniformly)

Q11.
a)
:
:
:
j) 10x2

Note for the paper setter:

1. The maximum duration to attempt the paper is 3 Hours.
2. Numbers of questions to be set are eleven (11) as per the above format.
3. Section A and B contain five questions of 5 marks each. However these questions may be divided into subparts.
4. Section C is compulsory and contains ten (10) sub-parts of two (2) marks each.
5. The maximum limit on numerical questions to be set in the paper is 35% while minimum limit is 20% except theoretical papers.
6. The paper setter shall provide detailed marking instructions and solution to numerical problems for evaluation purpose in the separate white envelopes provided for solutions.
7. The paper setters should seal the internal & external envelope properly with signatures & cello tape at proper place.
8. Log tables, charts, graphs, design data tables etc. should be specified, whenever needed. Use of Scientific calculator should be clearly specified.

MEC- 101 WIRELESS AND MOBILE DATA COMMUNICATION

L	T	P
3	1	0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Wireless Communication: Introduction, Cellular concept, Frequency reuse, Co-channel and adjacent channel interference, Cell splitting, Handover, Call processing.

Digital Cellular Mobile Systems: Introduction, GSM digital cellular standard: GSM services, GSM architecture, GSM Radio aspects, Security aspects, Handover, Call flow sequence in GSM, Evolutionary directions
CDMA Digital Cellular Standard: Services, Radio aspects, Security aspects, Traffic channels, Key features of IS- 95 CDMA system, Evolutionary directions.

SECTION-B

Equalization, Diversity and Channel Coding: Introduction, Training a Generic Adaptive Equalizer, Linear Equalizers, Non-Linear Equalization, Algorithm for Adaptive Equalization, Diversity Techniques, RAKE Receiver, Interleaving, Block codes, Convolution Codes and Turbo Codes.

Mobile Data Communications: Overview of circuit switched and packet switched data services on cellular networks, Wireless local area networks: Introduction, IEEE 802.11 wireless LAN, Support of mobility on the internet: Mobile IP

References:

1. Jochen Schiller, "Mobile Communications", Pearson Education
2. Raj Pandya, "Mobile and Personal Communication-System and Services", PHI
3. W. Stallings, "Wireless Communications and Network", Pearson Education
4. T.S. Rappaport, " Wireless Communications: Principles & Practice

MEC-102 OPTICAL COMMUNICATION SYSTEM

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

FIBER OPTIC GUIDES: Light wave generation systems, system components, optical fibers, SI, GI fibers, modes, Dispersion in fibers, Limitations due to dispersions, Fiber loss, non linear effects. Dispersion shifted and dispersion flattened fibers.
OPTICAL TRANSMITTERS AND FIBERS: Basic concepts, LED structures spectral distribution, semiconductor lasers, gain coefficients, modes, SLM and STM operation, Transmitter design, Reciever PIN and APD diodes design, noise sensititvity and degradation, Reciever amplifier design

SECTION-B

LIGHT WAVE SYSTEM: Coherent, homodyne and Hetrodyne keying formats, BER in synchronous and asynchronous recievers, sensitivity degradation, system performance, Multichannel, WDM, multiple access networks, WDM components, TDM, subcarrier and code division multiplexing.
AMPLIFIERS: Basic concepts, Semiconductor laser amplifiers Raman-and Brillouin-fiber amplifiers, Erbium doped-fiber amplifiers, pumping phenomenon, LAN and cascaded In-line amplifiers.

DISPERSION COMPENSATION: Limitations,post-and pre-compensation techniques, Equalizing filters, fiber soliton, Soliton based communication system design, High capacity and WDM soliton system.

Fiber Optic Network: Architecture of Fiber-Optic Networks, Network Management and the future.

References:
1. G. P. Agrawal, "Fiber Optic Communication Systems," 2nd Edition, John Wiley & Sons, New York, 2003.
2. Frenz and Jain, "Optical Communication System," Narosa Publication, New Delhi, 1995.
3. G. Keiser, Optical fiber communication Systems, Mc Graw Hill, New York, 2000
4. Frenz and Jain, Optical Communication systems and Components, Narosa Publications, New Delhi, 2000

MEC-103 VLSI DESIGN

L T P
3 1 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction to VHDL, Data objects and Data types, Operators, Entity and Architecture declaration, Introduction to Behavioural, Dataflow and Structural style of modeling.

Assignment statements, Sequential statements, Conditional statements, Concurrent statements, Case statements, Array and Records, Functions, Packages & Libraries.
VHDL modeling of combinational circuits such as Adders, Subtractors, Multiplexers, Encoders, Decoders, Code converters, Comparators and Implementation of Boolean functions using Behavioural, Dataflow and Structural style of modeling.

VHDL Modeling of sequential circuits such as Flip Flops, Shift registers, Counters etc.

SECTION-B

VLSI Design Flow, Design Methodologies, Abstraction Levels.

Design of NMOS inverter with resistive and active load, Design of CMOS inverter,Design of 2-input CMOS NAND gate, Design of 2-input CMOS NOR gate. CMOS Transmission gate.
Introduction to ROM, PLA, CPLDs and FPGA, FPGA arhitechture: SRAM based FPGAs, permanently programmed FPGAs. Structural details of Altera and XiLinx FPGAs.

Logic Implementation for FPGA's, Physical design for FPGAs, Introduction to Multi-FPGA systems.

References:

1. "A VHDL Primmer": Bhasker; Prentice Hall
2. "VDHL-Analysis & Modelling of Digital Systems": Navabi Z; McGraw Hill
3. "FPGA Based System Design": Wayne Wolf; Pearson Education.
4. "An Engineering Approach to digital design" William I. Fletcher; Prentice Hall
5. Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3rd Ed.
6.Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill (2008) 3rd ed.
7. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, Addision Wesley (1998) 2nd ed.

MEC-104 MICROCONTROLLERS AND EMBEDDED SYSTEMS

L T P
3 1 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: The Overview of 8051 Microcontroller Family, The Inside of 8051 Microcontroller, Pin Description of the 8051, Addressing Modes.

Instruction Set: Arithmetic, Logic and Single Bit Instructions, I/O instructions, etc.

Assembly Language Programming: I/O Programming, Timer/Counter Programming, Serial communication, Interrupts Programming.

SECTION-B

Introduction to Embedded Systems: An Embedded System, Processor in the System, Hardware Units, Software, and Embedded System Examples.

Processor and Memory Organization: Structural Units in a Processor, Processor Selection for Embedded System, Memory Map, Interfacing Processor, Memories and I/O Devices.

Devices and Buses: I/O Devices, Timer and Counting Devices, Serial and Parallel Communication Between Networked Multiple Devices Using I^2C, CAN, ISA, PCI and advanced I/O Buses.

Hardware-Software Co-design in an Embedded System: Embedded System Project Management, Design Issues in system Development Process, Design Cycle, Use of Target System and In-Circuit Emulator, Software tools for Development of Embedded System, Issues in Embedded System Design, Case Studies.

References:

1. Mazidi, "The 8051 Microcontroller and Embedded Systems, Pearson
2. Raj Kamal, "Embedded Systems," Tata McGraw Hill
3.Kenneth J. Ayala, "The 8051 Microcontroller," Penram International

MEC-105 ADVANCED DIGITAL SIGNAL PROCESSING

L T P
3 1 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Review of, classification of signals and systems, convolution, difference equations, correlation.

Fourier and Z Transforms: Properties of Fourier and Z transforms, Frequency analysis of discrete time signals and LTI Systems.
Discrete Fourier Transform: Definition and properties of DFT, Linear filtering methods using DFT, Frequency analysis of signals using the DFT.

Fast Fourier Transform: FFT algorithms and their applications, linear filtering approach to computation of the DFT.

SECTION-B

Implementation of Discrete Time systems: Structure of IIR and FIR systems, state space analysis and structures, Quantization of filter co- efficients.

IIR Filter Design: IIR filter design by Impulse invariance, Bilinear Transformation, Matched-z Transformation and Approximation of Derivatives Methods Characteristics of commonly used Analog Filters.

FIR Filter Design: Symmetric & Antisymmetric FIR filter design by Frequency Sampling, Using windows methods.

DSP Processors: Introduction to DSP Processors, Architecture TMS 320C54X and ADSP 2100 DSP processors.

Applications of DSP: Applications of DSP in Communications, speech processing, image processing, Biomedical and in Radars with case studies.

References:

1. *Johan G. Proakis and Dimitris G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications," PHI*
2. *N. G. Palan, "Digital Signal Processing," Tech Max Publications Pune*
3. *Nair, " Digital Signal Processing: Theory, Analysis and Digital Filter Design," PHI*
4. *Digital Signal Processing By Mitra*
5. *Oppenheim & Schafer, "Digital Signal Processing," PHI*

MEC-106 RESEARCH METHODOLOGY

L-T-P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Nature and objectives of research. Methods of Research: historical, descriptive and experimental
Alternative approaches to the study of the research problem and problem formulation. Formulation of hypotheses, Feasibility, prepration and presentation of research proposal

Introduction to statistical analysis : Probability and probability distributions; binomial, Poisson, exponential and normal distributions and their applications.
Sampling: Primary and secondary data, their collection and validation, methods of sampling: Simple random sampling, stratified random sampling and systematic sampling, Attitude Measurement land Scales: Issues, Scaling of attitude, deterministic attitudes, measurement models, summative models, multidimensional scaling.

SECTION-B

Regression and correlation analysis. Tests of significance based on normal., t and chisquare distributions. Analysis of variance. Basic Principles of design of experiments, completely randomized and randomized block designs.

.
Edition, tabulation & testing of hypotheses, interpolation of results, presentation, styles for figures, tables, text, quoting of reference and bibliography. Use of software for statistical analysis like SPSS, Mini Tab or MAT Lab, Report writing, preparation of thesis, use of software like MS Office.

REFERENCES:

1. C.R Kothari, Research Methodology, Wishwa Prakashan
2. P.G Triphati, Research Methodology, Sultan Chand & Sons, N.Delhi
3. Fisher, Design of Experiments, Hafner
4. Sadhu Singh, Research Methodology in Social Sciences, Himalya Publishers
5. Stoufferetal, Measurement & Prediction, Wiley, N.York
6. J.W Bames, Statistical Analysis for Engineers & Scientists, McGraw Hill, N.York
7. Donald Cooper, Business Research Methods, Tata McGraw Hill, N.Delhi

MEC-201 ANTENNA SYSTEM ENGINEERING

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

Section-A

Basic Concepts of Radiation: Radiation mechanism, Basic sources of Radiation, Current distribution on antennas, Basic Antenna parameters.

Analysis and Synthesis of Antennas: Vector potential, Antenna theorems and definitions, dipole, loop, reflector, slot antennas, types of linear arrays, current distribution in linear arrays, Antenna synthesis techniques.

Radiation From Apertures: Field equivalence principle, Rectangular and circular apertures, Uniform distribution on an infinite ground plane, Aperture fields of Horn antenna-Babinets principle, Geometrical theory of diffraction, Reflector antennas, Design considerations - Slot antennas.

Micro Strip Antennas: Radiation mechanisms, Feeding structure, Rectangular patch, Circular patch , Ring antenna. Input impedance of patch antenna, Microstrip dipole, Microstrip arrays.

SECTION-B

Smart Antennas: Spatial Radio Channel, Spatial processing for wireless systems: introduction, Vector channel impulse response & the Spatial signature, Spatial processing receivers, fixed beam forming networks, switched beam system, Adaptive antenna systems, Wide band smart antennas, Digital radio receiver & software radio smart antennas.

MIMO Communication Systems: Introduction, Basic Principle, Types: SIMO, MIMO, Space time block coding, SISO & MIMO Characteristics, Space time transmit diversity (STTD), MIMO Capacity gain, MIMO radio Channel model.

References :

1. *Joseph C. Liberti, Theodore S. Rappaport-"Smart Antennas for Wireless Communications IS95 and third generation CDMA Applications", Prentice Hall, Communications Engineering and Emerging Technologies Series, 2007*
2. Kraus J.D., "Antennas for all Applications", III Edition, TMH, 2005
3. Collin R.E. and Zucker F.- "Antenna Theory" Part I, Tata McGraw Hill, 2005
4. Balanis A., "Antenna Theory Analysis and Design", John Wiley and Sons, New York, 2002.

MEC-202 DIGITAL IMAGE PROCESSING AND ANALYSIS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction and Digital Image Fundamentals: Fundamental steps in Image processing, Examples of fields that use digital Image processing, Image sensing and acquisition, Image Sampling and quantization, some basic relationships like neighbor's connectivity, distance measure between pixels.
Image Transforms: Discrete Fourier transform, some properties of two-dimensional Discrete Fourier transform, Fast Fourier transform, Inverse FFT.

Image Enhancement: Some basic Intensity transformation functions, Histogram processing, Smoothing using Spatial filters and frequency domain filters, Sharpening using spatial filters and frequency domain filter,
Image Restoration: Image Degradation model, Noise Models, Restoration in spatial domain: Mean filter, Order statistic.

SECTION-B

Image Compression: Coding Inter-pixel and Psycho visual redundancy, Image Compression models, Error free compression: Huffman, Arithmetic, Runlength, Lossy Compression: Block Transform Coding based on DCT.
.

Morphological Image Processing and Image Edge Detection: Erosion and dilation, morphological algorithms, gray scale morphology. Detection of discontinuities, Edge linking and boundary detection, thresholding, Region Orientation Segmentation.
and Laplacian of Gaussian edge detector.

Reference Books:

1. Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", AWL.
2. Andrew, "Fundamentals of digital image processing", PHI
3. A.K. Jain," Fundamentals of Digital Image Processing", Pearson Education.
4. W. K. Pratt," Digital Image Processing".
5. Ramesh Jain, Brian G. Schunck, "Machine Vision", TMH.

MEC-203 INFORMATION THEORY AND CODING

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Information, Entropy, Shanon's noiseless coding theorem, Source Coding, Channel Capacity, Shanon's Channel Capacity Theorem. Sampling Theorem: Practical Aspects and Signal Recovery.

Waveform Coding: PCM Channel Noise and error Probability. DPCM and DM Coding Speech at Low Bit Rates Prediction and Adaptive Filters. Base Band Shaping for data Transmission. PAM signals and their Power Spectra. Nyquist Criterion, ISI and eye Pattern Equalization.

SECTION-B

Binary and M-ary Modulation Techniques: Coherent and Non Coherent Detection. Error probability and Bandwidth Efficiency. Bit error analysis Using Orthogonal Signaling.

Channel Coding and Decoding Techniques: Channel Coding- Block Codes, Cyclic Codes and Convolution Codes, Decoding, Viterbi Decoding Algorithm. Trellis Codes.

References:

1. *Digital Communication Techniques: Signal Design and Detection by Simon, PHI*
2. *Principles of Communication Systems By Taub and Shilling, Tata Mc-Graw Hill*
3. *Digital and Analog communication By Couch, Pearson*
4. *Communication Systems Engineering, By John G. Proakis Masoud Salehi, Pearson*

MEC-204 EMI AND EMC TECHNIQUES

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Aspects of EMC with Examples, Common EMC Units, EMC Requirements for Electronic Systems, Radiated Emission, Conducted Emission, ESD.

EMC Design: Application of EMC Design, wires, PCB Lands, Component Leads, Resistors, Capacitors, Inductors, ferrites, Electromechanical Devices, Digital Circuit Devices.

SECTION-B

Application Design: Mechanical Switches, Simple emission Model for Wires and PCB Lands, Lice Impedance Stabilization Network (LISN), Power Supply Filters, Power Supplies including SMPS, Three Conductor lines and Crosstalk, Shielded Wires, Twisted Wires, Multiconductor Lines and Effect of incident fields, Shielding and Origin effect.

Immunity and Protection in Design: Prevention of ESD event, its hardware and immunity, System Design for EMC, Grounding, System Configuration, PCB Design.

References:

1. *The Technician's EMI Handbook: Clues and Solutions By Joseph Carr*
2. *Grounding and Shielding Techniques By Ralph Morrison*
3. *EMC for Product Designers, Third Edition By Tim Williams*
4. Printed Circuit Board Design Techniques for EMC Compliance By Mark I. Montrose

MEC-205 SEMICONDUCTOR DEVICES AND MODELING

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Semiconductors, Integrated Circuit Fabrication Technology, Charge Transport in Semiconductors, Applications of PN junction, Bipolar Junction Transistor and Thyristers, JFET and MOSFET.

Diode and Transistor Modeling: Integrated Circuits Diodes and Transistors, Current Voltage Characteristics, Ebersmoll Model and Gummel-Poon Model of Bipolar Transistors. Current Gain, Early Effect and High Level Injection, 2-D effect, Transient Parameters.

SECTION-B

MOSFET Modeling: MOSFETs, Analysis of MOSFET Parameters, Short Channel and Narrow Width Effects, Hot Electron Effects, MOSFET Models.

FET Modeling: FETs, Modulation Doped FETs, HEMTs, Heterojunctions and HBTs, Microwave and Optonic Devices, Outline of Numerical Approach to 2D and 3D Device Models.

References:

1. *Semiconductor Devices: Modeling and Technology By Das Gupta PHI*
2. *Semiconductor Devices By Kano Pearson Education*

MEC-206 ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC SYSTEMS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Biological neuron physiology, brain specifications, artificial neural networks, historical development, ANN characteristics, terminology and topology of neural networks, neuron model: McCulloh, Perceptron, ADALINE and MADALINE, Learning in artificial neural networks: supervised learning, unsupervised learning, reinforced learning, competitive learning, Learning Rules: Delta learning, Perception learning, Widrow Hoff learning, Correlation learning, Winner-take-all learning and Hebbian learning.

Neural Network Paradigms: Feed-forward and feedback neural networks, Back-propagation learning algorithm and its mathematical analysis, Hopfield model and its mathematical analysis, Kohonen model and its applications, introduction to radial basis function, applications of ANN.

SECTION-B

Fuzzy Logic Fundamentals: Basic concepts, propositional logic, linguistic variable, membership functions, operations and rules of fuzzy sets, fuzzy logic, Product, Composition, fuzzy rule generation, IF THEN ELSE Rule, Approximate reasoning, de-fuzzification.

Fuzzy System Design: Fuzzy system design, conventional control system vs. fuzzy logic control system, fuzzy logic control vs. PID control, industrial applications of fuzzy logic control, introduction to fuzzy neural networks and fuzzy neural control.

References:

1. Stamatios V. Kartalopoulos, "Understanding Neural Networks and Fuzzy Logic," PHI
2. B. Yegnarayana, "Artificial Neural Networks," PHI
3. Ahmad M. Ibrahim, Introduction to Applied Fuzzy Electronics, PHI
4. T. J. Ross, "Fuzzy Logic with Engineering Applications", McGraw-Hill
5. J Nie & D Linkers, "Fuzzy Neural Control", PHI
6. J.M.Zurada, 'Iintroduction to Artificial Neural system", Jaico Publishers.

MEC-207 MEMS AND MICROSYSTEMS TECHNOLOGY

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Introduction to Microsensors and MEMS, Evolution of Microsensors and MEMS, Microsensors and MEMS Applications.

Microelectronics: Microelectonic Technologies for MEMS, Micromachining Technology: Surface and Bulk Micromachining, Micromachined Microsensors- Mechanical, Interial, Chemical, Acoustic.

SECTION-B

Microsystems: Micosystems Technology, Integrated Smart Sensors and MEMS, Interface Electronics for MEMS.

Applications and Simulators: MEMS Simulators, MEMS for RF Applications, Bonding and Packaging of MEMS, Future Trends.

References:

1. MEMS and Microsystems Design and Manufacture By Hsu, Tai- Ran, Mac Graw Hill
2. Introduction ot Microelectromechanical Systems Engineering, By Nadim Maluf and Kirt Williams, Artech House Publishing
3. MEMS Mechanical Sensors,"By Steve Beeby and Graham Ensel and Michael Kraft and Neil White, Artech House Publishin

MEC-208 TELECOMMUNICATION SWITCHING SYSTEMS AND NETWORKS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Evolution of Telecommunications, basics of switching system, Telecommunication Networks. Strowger Switching Systems, Crossbar Switching, Electronic Space Division Switching.

Data Transmission: Speech Digitization and Transmission, Time Division Multiplexing Switching, Frequency Division Multiplexing Switching, Code Division Multiplexing Switching, Applications of Optical Fiber Systems in Telecommunications.

SECTION-B

Data Networks: Data Transmission in PSTNs, switching Techniques for Data Transmission, Data Communication Architecture, Link to Link and End to End Layers, Satellite Based Data Networks, LAN, MAN, Fiber Optic Networks, Data Network Standards, Protocol Stacks and Internetworking.

Telephone Networks: Subscriber Loop Systems, Transmission Plan and Systems, Numbering and Charging Plan, Signalling Techniques, cellular Mobile Telephony.

Traffic Engineering: Network traffic Load and Parameters,Grade of servicing and Blocking Probability, Modelling Switching Systems, incoming Traffic and service Time Characteristics, blocking Models and Loss Estimates, Delay Systems.

Integrated Services Digital Networks(ISDN): Network and Protocol Architecture, Transmission Channels, User Network Interfaces, Signalling, Numbering and addressing, ISDN Standards, Expert Systems in ISDN, Broadband ISDN.

References:

1. Telecommunicaion Switching Systems and Networks By Thiagarajan Viswanathan, PHI
2. Telecommunication Switching,Traffic and Networks, By Flood, Pearson
3. ISDN and Broadband ISDN By Stallings, PHI

MEC-209 PROGRAMMABLE LOGIC CONTROLLER

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

PLC Basics: An Overall Look at PLCs, The PLC: A Look Inside, PLC Programming procedures, Devices to Which PLC Input and Output Modules are Connected.
Basic PLC Programming: Programming On/Off Inputs to Produce On/ Off Outputs, Relation of Digital Gate Logic to Contact/ Coil Logic, creating Ladder Diagram from Process Control Descriptions.Ladder diagram of various gates, De Morgan's Theorem

Basic PLC Functions: Registers, Timer Functions, Counter Functions, Arithmetic Functions, Comparison Functions, Numbering Systems and Number Conversion Functions.

SECTION-B

Data Handling Functions: PLC Skip and Master Control Relay Functions, Jump Functions, PLC Data Move Systems and data Handling Functions.

PLC Functions Handling with Bits: Digital Bit Functions, Sequencer Functions and Matrix Functions.

Advanced Instructions: Comparison , Data movement , Logical , Mathematical & Special mathematical , data handling, program flow control , PID instructions.
Advanced PLC Functions: Analog PLC Operations, PID Control of Continuos Process, Networking of PLCs, Factors to Consider in Selecting a PLC.

References:

1. John W. Webb, "Programmable Logic Controllers: Principles and Applications, PHI.
2. Gary Dunning, "Introduction to PLCs, Thomson Delmar
3. Jay. F. hooper, "Introduction to PLCs"

MEC 210 NANOELECTRONICS DEVICES ENGINEERING

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Nano, Size matters, Fundamental Science Behind Nanotechnology, Tools of Nanosciences.

Silicon Nanoelectronics and Ultimate CMOS Microelectronic Transistor: Structure, operation, Obstacles to Miniaturization: Structure and Operation of a MOSFET, Obstacles to Further Miniaturization of FETs.

SECTION-B

Solid State Quantum Effect and Single-electron Nanoelectronic Devices: Island, Potential Wells, and Quantum effects, Resonant Tunneling Devices, Distinction Among Types of nanoelectronic devices.

Devices: Other Energetic Effects, Taxonomy of Nanoelecronic Devices, Drawbacks and Obstacles to Solid-State Nanoelectronic Devices.

Molecular Electronics: Molecular Electronic Switches Devices, Background of Molecular Electronics, Molecular Wires, Quantum- effect Molecular Electronic Devices, Electromechanical Molecular Electronic Devices. Introduction to nanolithography devices.

References:

1. *Ratner, "Nanotechnology, A Gentle Introduction to Next Big Idea," Pearson*
2 *Overview of Nanoelectronic Devices, IEEE Proceedings.*
3. *Silicon Nanoelectronics By Shunri Oda*

MEC-211 PARALLEL COMPUTING FUNDAMENTALS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Evolution, Parallel Processing Terminology, Data and Control Parallelism, Pipelining, Flynn's Taxonomy, Speedup, Scaled Speedup, and Parallelizability
PRAM Model, Parallel Algorithms.

Multiprocessors: Processor Arrays, Multiprocessors and Multi-computers. Processor Organizations, Processor arrays, Multiprocessors- UMA, NUMA, Multi-computers

Parallel Processing: Instruction level Parallel Processing, Pipelining of processing elements, Pipelining Limitations, Superscalar Processors, Very Long Instruction Word Processor

SECTION-B

Interconnection Networks: Basic Communication Operations, Interconnection Networks

Mapping and Scheduling: Embedding of task graphs in processor graphs, Dilation, Load Balancing on Multicomputers, Static Scheduling techniques, Deterministic and Non-deterministic models, Prevention of deadlocks

Performance Evaluation of Parallel Computers: Basics, Sources of Parallel overhead, Speed -Up Performance Laws, Amdhal's law, Scalability Metric, Performance Measurement Tools.

References:

1. Michael J. Quinn, "Parallel Computing, Theory & Practice", McGraw-Hill
2. V Rajaraman & C S R Murthy, "Parallel Computers, Architecture and Programming", PHI
3. A. Grama, "Introduction to Parallel Computing ", Pearson Education
4. Hwang & Briggs F.A., "Computer Architecture and Parallel Processing"

MEC –212 SPEECH PROCESSING

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction: Fundamentals of Digital Speech Processing, Digital Models of the Speech Signal.

Speech Processing Models: Time Domain Models of Speech Processing, Digital Representation of Speech Waveform.

SECTION-B

Fourier Analysis and Homomorphic Speech Processing: Short-Time Fourier Analysis, Homomorphic Speech Processing.

Coding and Digital Speech Processing: Linear Predictive Coding of Speech, Digital Speech Processing for Man-Machine- Communication by Voice.

References:

1. *Rabiner, "Digital Processing of Speech Signals," Pearson*
2. *Thomas, 'Discrete Time Speech Signal Processing," Pearson*

MEC- 213 COMPUTER SYSTEM ARCHITECTURE

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Basic Computer Organization: Introduction, Organization & Architectural classification, Computer Evolution and Performance, computer System Buses, registers & stacks, ALU, CPU, Control Unit, Hardwired and Micro programmed Control.

CPU Instruction Sets: Characteristics, Functions, Addressing modes and Formats, CPU Structure, Processor & Register Organization, RISC and Superscalar Processors, PowerPC, Pentium processors etc.
Computer Arithmetic: Integer & Floating Point Arithmetic.

SECTION-B

Memory and I/O Devices: Internal & External memory, Virtual & High-Speed memories, I/O Devices & Modules, Programmed & Interrupt driven I/O, DMA.

Parallel Processing and Pipelining: Introduction, Parallelism in uniprocessor system, Memory interleaving, Pipelining and vector processing, Instructions and arithmetic pipelines, Array processor, parallel processing algorithms.

References:

1. John P. Hayes, "Computer Architecture and Organization", McGraw-Hill
2. Stallings, "Computer Organization and Architecture", Pearson Education
3. M. M. Mano, "Computer System Architecture", PHI
4. Patterson and Hennessy, "Computer Architectures", Morgaon Kauffman

MEC-214 MICROELECTRONICS TECHNOLOGY

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Crystal Growth and Wafer Preparation: Materials for formation of crystal, Electronic-Grade Silicon, Czochralski Crystal Growth, Silicon Shaping, Horizontal Bridgeman Method, Distribution of dopants, Zone refining, Silicon Float Zone process, Si-Wafer preparation.
Epitaxial and Oxidation: Silicon on insulators, Epitaxial growth, Techniques used for Epitaxial growth such as LPE, VPE, MBE. Growth Mechanism and Kinetics, Thin Oxides, Oxidation Techniques and Systems, Effect of impurities on the oxidation rate, Preoxidation Cleaning, Masking properties of SiO2.

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography, Photolithography Process (Lift off technology, Fine line photolithography), Pattern Generation/Mask making, Contact and Proximity printing, Photoresists.
Etching Techniques & Film Deposition: Wet/Dry etching, Reactive Plasma etching techniques and applications, Size Control and Anisotropic Etch Mechanisms, Deposition Processes, Polysilicon and Silicon Dioxide Layer Deposition.

SECTION-B

Diffusion: Models of Diffusion in Solids, Fick's One-Dimensional Diffusion Equations, Atomic Diffusion Mechanisms, Basic diffusion process (Diffusion equation, Diffusion profiles), Extrinsic diffusion, Lateral Diffusion.
Ion Implantation: Range Theory, Implantation Equipment, Annealing, Ion Implantation Process (Ion distribution, Ion stopping), Implant Damage and Annealing process (Furnace and RTA).

Metallization: Metallization Applications, Metallization Choices, Physical vapor Deposition, Patterning.
VLSI Process Integration: Introduction, Various IC Packaging methods and Materials, Isolation Techniques, Chip Testing, Wire Bonding techniques, Flip Chip technique, NMOS IC Technology, CMOS IC Technology, Bipolar IC Technology.

References:

1.DA. And Eshraghian K "Basic VLSI design systems & circuits" PHI.
2.Geigar BR, Allen PE & Strader ME, "VLSI design techniques for analog & digital circuit" McGraw -Hill.
3.S.M. Sze, "VLSI Technology" McGraw-Hill.
4.S.K.Gandhi, "VLSI Fabrication Principles" John Wiley & Sons.
5.D. Nagachaudhary, "Introduction to Microelectronics Technology," Dorling Kindersley.
6.K.R.Botkar, "Integrated Circuits" Khanna Publishers.

MEC-215 ADVANCED DIGITAL SYSTEM DESIGN

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Minimization and Design of Combinational Circuits: minimization with theorems, Karnaugh Map, Variable-entered mapping and Tabulation method.
MSI and LSI Circuits and Applications: Arithmetic circuits, Comparators, Multiplexers, Code converters, EXOR AND-OR-INVERT Gates, Wired Logic, TRI -STATE BUS SYSTEM, Propagation Delay.

SEQUENTIAL MACHINE FUNDAMENTALS: Need for sequential circuits, Distinction between combinational and sequential circuits, Concept of memory, Binary Cell, Classification of sequential machines, Flip-Flop, Design of clocked Flop-Flops, Conversion of Flip- Flops.

TRADITIONAL APPROCH TO SEQUENTIAL ANALYSIS AND DESIGN: State Diagram, Analysis, Design of Synchronous sequential circuits, State Reduction, Minimizing the next state decoder, Out put decoder design, Counters, Design of Single Mode, Multi Mode Counters, Ring Counters. Shift Registers.

SECTION-B

MULTI INPUT SYSTEM CONTROLLER DESIGN: System Controllers**,** timing and frequency considerations, MDS Diagram Generation, Synchronizing to systems and choosing controller Architecture, State Assignment ,Next State Decoder, Next State decoder maps, Output Decoder, Control and display.

SYSTEM CONTROLLER UTILIZING COMBINATION MSI/LSI CIRCUITS: Using the MSI decoders in system controller, MSI multiplexes in system controller, Indirect- Addressed Multiplexer Configuration.

ASYNCHRONOUS FINITE-STATE MACHINES: Introduction, Asynchronous Analysis, The Design of Synchronous Machines, Cycles and races, Hazards, Read only memories, ROM'S PROMS and applications, Using the ROM random logic, Programmed Logic arrays, Applications of PLA

References:
1. *Wiilian I Fletcher, "An Engineering Approach to Digital Design," PHI*
2. *Morris Mano and Charles R. Kime, "Logic and Computer Design Fundamentals,"*

MEC-216 ADVANCED MICROPROCESSORS AND INTERFACING

L T P
3-1-0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Introduction to Microprocessors: Types of Processors, 16 Bit Microprocessors, Features and Internal Architecture of Microprocessor 8086, Register Organization and Block Diagram of 8086 Microprocessors. Addressing Modes of 8086, Pin Configuration of 8086, Maximum and Minimum Mode, 8284 Clock Generator, 8288 Bus Controller.

Instruction Set: 8086 Instruction Groups, Addressing Mode Byte, Segment Register Selection, Segment Override and 8086 Instructions.

Debug and Assembler: Debug Commands, Assembler Directives, Operators, Assembly Language Programming of 8086.

SECTION-B

Memory and I/O Interfacing: Interfacing EPROM and RAM to 8086. I/O Interfacing Techniques. Interfacing of PPI 8255, Programmable DMA Controller 8237, Programmable Interrupt Controller 8259.

32-Bit Microprocessors: Introduction, features, architectures and addressing modes of 386, 486 and Pentium Microprocessors.

References:

1. Badri Ram, "Advanced Microprocessors and Interfacing," Tata McGraw hill
2. Gilmore, "Microprocessor Principles and Applications," Tata McGraw Hill
3. Walter A. Tribel and Avtar Singh, "8088 and 8086 Microprocessor, PHI
4. B. Bray, "Advanced Microprocessor and Interfacing", PHI

MEC-217 MULTIMEDIA COMPRESSION TECHNIQUES

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

INTRODUCTION: Brief history of data compression applications, Overview of information theory, redundancy. Overview of Human audio, Visual systems, Taxonomy of compression techniques. Overview of source coding, source theory, rate distribution theory, vector quantisation, structure quanitizers. Evaluation techniques-error analysis and methodologies.

TEXT COMPRESSION: Compact techniques-Huffmann coding-arithmatic coding-Shannon-Fano coding and dictionary techniques- LZW family algorithms. Entropy measures of performance-Quality measures.

AUDIO COMPRESSION: Audio compression techniques-frequency domain and filtering-basic subband coding-application to speech coding-G.722-application to audio coding-MPEG audio, progressive encoding for audio-silence compression, speech compression techniques-Vocoders.

SECTION-B

IMAGE COMPRESION: Predictive techniques-PCM, DPCM, DM. Contour based compression-quadtrees, EPIC, SPIHT, Transform coding, JPEG, JPEG-2000, JBIG.

VIDEO COMPRESSION : Video signal representation, Video compression techniques-MPEG, Motion estimation techniques- H.261.Overview of Wavelet based compression and DVI technology, Motion video compression, PLV performance, DVI real time compression.

References:

1. *Mark Nelson,Data compression book, BPB Publishers,New Delhi,1998*
2. Sayood Khaleed, Introduction to data compression, Morgan Kauffman ,London,1995
3. Watkinson,J.Compression in video and audio, Focal press,London.1995
4. Jan Vozer,Video compression for multimedia,AP profes,NewYork,1995.

MEC-218 MICROWAVE INTEGRATED CIRCUITS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

MICROSTRIPS LINES, DESIGN, ANALYSIS: Introduction, types of MICs and their technology, Propagating models, Analysis of MIC by conformal transformation, Numerical analysis, Hybrid mode analysis. losses in Microstrip, Introduction to slot line and coplanar waveguide.
COUPLED MICROSTRIP, DIRECTIONAL COUPLERS AND LUMPED: Introduction to coupled Microstrip, Even and odd mode analysis, Directional couplers, branch line couplers, Design and Fabrication of Lumped elements for MICs, Comparison with distributed circuits.

NON-RECIPROCAL COMPONENTS AND ACTIVE DEVICES FOR MICS: Ferromagnetic substrates and inserts, Microstrip circulators, Phase shifters, Microwave transistors, Parametric diodes and Amplifiers, PIN diodes, Transferred electron devices, IMPATT, BARITT, Avalanche diodes, Microwave transistors circuits.

SECTION-B

MICROSTRIP CIRCUIOT DESIGN AND APPLICATIONS: Introduction, Impedance transformers, Filters, High power circuits, Low power circuits, MICs in satellite and Radar

MMIC TECHNOLOGY: Fabrication process of MMIC, Hybrid MICs, Configuration, Dielectric substances, thick and thin film technology, Testing methods, Encapsulation and mounting of Devices.

References:
1. Hoffman R. K. "HandBook of Microwave intergrated circuits", Artech House, Boston,1987.
2. Gupta K.C and Amarjit Singh,"Microwave Intergrated circuits" John Wiley, New York,1975.

MEC-219 GLOBAL TRACKING AND POISIOTIONING SYSTEM

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

INTRODUCTION: Satelites, Introduction to Tracking and GPS System, Applications of Satelite and GPS for 3D position, Velocity, determination as function of time, Interdisciplinary application (eg,.Crystal dynamics, gravity field mapping, reference frame, atmospheric occulation)Basic concepts of GPS. Space segment, Control segment, user segment, History of GPS constellation, GPS measurement charecteristics, selective availability(AS), antispoofing (AS).

ORBITS AND REFERENCE SYSTEMS: Basics of satelite orbits and reference systems-Two-body problem, orbit elements, timre system and time transfer using GPS, coordinate systems, GPS Orbit design, orbit determination problem, tracking networks, GPS force and measurement models for orbit determination, orbit broadcast ephemeris, precise GPS ephemeris, Tracking problems

GPS MEASUREMENTS: GPS Observable-Measurement types(C/A Code,P-code,L1 and L2 frequencies for navigation, pseudo ranges),atmospheric delays(tropospheric and ionospheric),data format(RINEX),data combination(narrow/wide lane combinations, ionosphere-free combinations single, double, triple differences), undifferenced models, carrier phase Vs Intergrated Doppler, integer biases, cycle slips, clock error.

SECTION-B

PROCESSING TECHNIQUES: Pseudo range and carrier phase processing, ambiguity removal, Least square methods for state parameter determination, relation positioning, dilution of precision.

GPS APPLICATIONS: Surveying, Geophysics, Geodsey, airborne GPS, Ground transportation, Spaceborne GPS orbit determination, attitude control, meteorological and climate research using GPS.

References:

1. *B. Hoffman - Wellenhof, H. Lichtenegger and J. Collins, "GPS: Theory and Practice ", 4th revised edition, Springer, Wein, New york, 1997*
2. *A. Leick,"GPS Satelite Surveying",2nd edition, John Wiley & Sons, NewYork,1995*
3. *B. Parkinson, J. Spilker, Jr.(Eds),"GPS: Theory and Applications", Vol. I & Vol.II,AIAA,370 L 'Enfant Promenade SW,Washington,DC20024,1996*
4. *A. Kleusberg and P. Teunisen (Eds),GPS for Geodesy,Springer-Verlag,Berlin,1996*
5. *L. Adams, "The GPS.A Shared National Asset, Chair, National Accademy Press, Washington, DC, 1995.*

MEC-220 COMMUNICATION NETWORK SECURITY

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

CONVENTIONAL ENCRYPTION: Introduction, Conventional encryption model, Steganography, Data Encryption Standard, block cipher, Encryption algorithms, confidentiality, Key distribution.

PUBLIC KEY ENCRYPTION AND HASHING: Principles of public key cryptosystems, RSA algorithm, Diffie-Hellman Key Exchange, Elliptic curve cryptology, message authentification and Hash functions, Hash and Mac algorithms, Digital signatures.
IP SECURITY: IP Security Overview, IP security Architecture, authentification Header, Security payload, security associations, Key Management.

SECTION-B

WEB SECURITY: Web security requirement, secure sockets layer, transport layer security, secure electronic transaction, dual signature.

SECURITY SYSTEM: Intruders, Viruses, Worms, firewall design, Trusted systems, antivirus techniques, digital Immune systems.

References:

1. *William Stallings,"Cryptography and Network security", 2nd Edition ,Prentice Hall of India, New Delhi, 1999*
2. *Baldwin R and Rivest. R. "TheRC5,RC5-CBC,TC5-CBC-PAD and RC5-CT5 Algorithms,RFC2040",October1996.*

MEC-221 RF SYSTEM DESIGN

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

INTRODUCTION: RF circuits, Impedance matching and Quality factor, Efficiency, Amplifiers, RF preamplifiers , filters, Frequency converters, Mixers, Radio receivers.
OSCILLATORS AND PLL: Relaxation oscillators, Series resonant oscillators, Negative resonant oscillators, Oscillator dynamics, Stability, oscillator noise, Design examples, phase locked loops-loop dynamics, analysis, Frequency synthesizers.

AMPLIFIERS AND POWER SUPPLIES: Amplifier specifications-gain,bandwidth and impedance, stability, Amplifier design, Noise considerations class C class D amplifiers High power amplifiers, Rectifiers, Switching converters, Boost and Buck circuits.

SECTION-B

COUPLERS AND WAVEGUIDE CIRCUITS: Directional coupling, Hybrids, Power combining, transformer equivalent circuits, Double tuned transformers, Transformers with magnetic and iron cores. Transmission lines, transformers Baluns, Waveguides, matching in wave guide circuits, Waveguide junctions, coaxial lines, resistance impedance bridge, standing waves.

MODULATION AND DETECTION CIRCUITS: AM, High level modulation, Digital to analog modulation, SSB, Angle and frequency modulation, Diode detectors, FM demodulators-Design. power detectors. Measurement of power, Voltage and Impedance. Swept frequency impedance measurements

References:

1. Jon B. Hagen, Radio Frequency Electronics, Cambridge university press,Cambridge,1996
2. James Hardy,"High Frequency Circuit Design", Resto Publishing Co.,NewYork,1979
3. Ian Hickman,"RF HandBook" Butter Worth Heinemann Ltd.,Oxford,1993.
4. Ulrich L. Rohde, T.T.N.Bucher,"Communication Recievers",Mc Graw Hill, New York,1998.
5. R. Ludcoig 'RF Circuit Design' Pearson Asia Education and P. Bretchko, New Delhi.2000.

MEC- 222 DATA AND COMPUTER COMMUNICATION NETWORKS

L T P
3- 1- 0

Maximum Marks: 50 **Maximum Time: 3 Hrs.**
Minimum Pass Marks: 40%

Instructions for paper-setter: The question paper will consist of three sections A, B, and C. Sections A and B will have four questions each from the respective sections of the syllabus and each question will carry five marks. Section C will have one question with 10 short answer /objective type parts, which will cover the entire syllabus uniformly and each part will carry 2 marks.
Instructions for candidates: Candidates are required to attempt three questions each from sections A and B of the question paper and the question in section C is compulsory.

SECTION-A

Data Communication Techniques: Synchronous-Asynchronous Transmission, Digital Transmission, Transmission Media, Impairments, Data encoding Techniques

Communication Networks: Circuit switching, Message switching, Packet Switching. X.25, LAN Technologies, Virtual Circuits

Network Reference Models: OSI and TCP/IP, Layered architecture

Data Link Layer: Design issue, framing, error control, flow control, HDLC, SDLC, data link layer in the Internet (SLIP, PPP)

Network Layer: Routing Algorithms, shortest path, distance vector routing, Link state routing, and multicast routing. Congestion control, traffic shaping, leaky bucket, token bucket, choke packets, load shedding, internetworking- connection oriented and connectionless, fragmentation, internet architecture and addressing, IP protocol, ICMP, APR, RARP, OSPF, BGP, CIDR, IPv6.

SECTION - B

Transport and Session Layer: Transport Service, quality of service, connection management, addressing, flow control and buffering, multiplexing, Internet transport protocols- TCP and UDP, Session layer- Dialogue management, synchronization and remote procedure call.

Presentation Layer: date representation, data compression, network security and cryptography.
Application Layer: DNS, SNMP, Telnet, TFTP, NFS E- mail, SMTP and World Wide Web

References:

1. A. S. Tanenbaum, "Computer Networks", Pearson Education
2. W. Stallings," Data and Computer Communications", PHI
3. J.F. Kurose, K.W. Ross, "Computer Networking: A Top-Down Approach featuring the Internet", Pearson Education
4. L.L. Peterson, B.S. Davie, "Computer Networks: A Systems Approach", Pearson Education

MEC-301 ELECTRONICS ENGINEERING LAB

Each student will be required to complete a course on Lab Work comprising of advanced Experiments related to Electronics Engineering. The experiments in the Lab Work will be decided by the concerned teacher/section-in charge. The student will be required to complete the prescribed Lab Course and other requirements related to evaluations of the Practical Course. The evaluation will be done by the committee of examiners constituted by Head of Department.

MEC-302 SELF STUDY AND SEMINAR

L-T-P
0- 0- 6

Each student will be required to prepare a Seminar Report and present a Seminar on a topic in any of the areas of modern technology related to Electronics Engineering including interdisciplinary fields. The topic/title will be chosen by the student in consultation with the Faculty Advisor allocated to each student. The student will be required to submit the Seminar Report and present a talk to an audience of Faculty/Students in open defense in front of the Seminar Evaluation Committee having Faculty Advisor as one of its members. The Head of Department will constitute the Seminar Evaluation Committee.

MEC -303 PROJECT

L-T-P
0- 0- 6

Each student will be required to complete a Project and submit a Project Report on a topic on any of the areas of modern technology related to Electronics Engineering including interdisciplinary fields. The title and objectives of the Project will be chosen by the student in consultation with the Project Guide allocated to each student. The student will be required to present a talk to an audience of Faculty/Students in open defense in front of the **Project Evaluation Committee** having Project Guide as one of its members. The Head of Department will constitute the Project Evaluation Committee for the purpose of evaluation for internal assessment.

MEC-401 DISSERTATION

Each student will be required to complete a Dissertation and submit a written Report on the topic on any of the areas of modern technology related to Electronics Engineering including interdisciplinary fields in the Final semester of M.Tech. course. The title and objectives of the Dissertation will be chosen by the student in consultation with the Supervisor (s) and the same will be required to be defended by the student in open defense in front of the **Dissertation Monitoring Committee** approved by the Head of Department. The title and objectives will be approved by the Dissertation Monitoring Committee having main Supervisor as one of its members. The progress will also be monitored at weekly coordination meetings with the Supervisor (s). The student will be required to present a talk to the gathering in open defense in front of the Dissertation Monitoring Committee having main Supervisor as one of its members. The Dissertation Monitoring Committee will be constituted by Head of Department for the purpose examining the suitability of the work carried out by the student in the Dissertation for its evaluation by the external examiner. The Dissertation will be sent to the External Examiner for its evaluation only after its due approval by the Dissertation Monitoring Committee. The external evaluation will be done jointly by the main Supervisor and external examiner appointed by the Head of Department. The dissertation (non-credit course) will be either approved or rejected. The external examiner will evaluate the dissertation and the viva-voce will be fixed by the Head of Department. After Viva-voce, the examiners (internal and external) will approve/reject the dissertation. In case, the dissertation is rejected, the candidate will rework and resubmit the dissertation. The dissertation will be again be evaluated jointly by the same external examiner and the Main Supervisor.